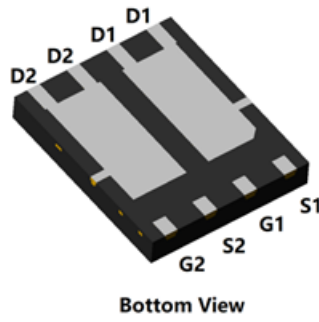
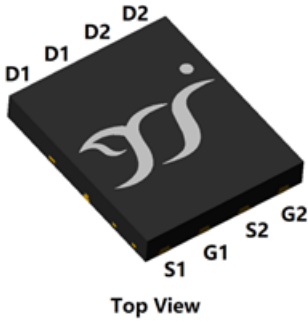
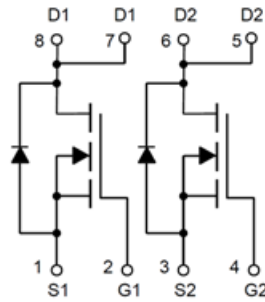


N-Channel Enhancement Mode Field Effect Transistor



DFN5060-8L



Product Summary

- NMOS (Die1)**
- V_{DS} 30V
 - I_D 40A
 - $R_{DS(ON)}$ (at $V_{GS}=10V$) <9.2mohm
 - $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <14.5mohm
- NMOS (Die2)**
- V_{DS} 30V
 - I_D 40A
 - $R_{DS(ON)}$ (at $V_{GS}=10V$) <9.2mohm
 - $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <14.5mohm

- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	N-Die1	N-Die2	Unit
Drain-source Voltage	V_{DS}	30	30	V
Gate-source Voltage	V_{GS}	± 20	± 20	V
Drain Current	I_D	$T_C=25^\circ C$	40	A
		$T_C=100^\circ C$	25	
Pulsed Drain Current ^A	I_{DM}	140	140	A
Total Power Dissipation	P_D	$T_C=25^\circ C$	21	W
		$T_C=100^\circ C$	8.4	
Total Power Dissipation	P_D	5	5	W
Single Pulse Avalanche Energy ^B	E_{AS}	49	49	mJ
Thermal Resistance Junction-to-Case ^C	$R_{\theta JC}$	6	6	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^C	$R_{\theta JA}$	25	25	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD40N03A	F1	YJGD40N03A	5000	10000	100000	13" reel



■ NMOS (Die1/Die2) Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =15A		7.2	9.2	mΩ
		V _{GS} = 4.5V, I _D =10A		11	14.5	
Diode Forward Voltage	V _{SD}	I _S =15A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				40	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz		1015		pF
Output Capacitance	C _{oss}			201		
Reverse Transfer Capacitance	C _{rss}			164		
Gate resistance	R _g	f=1MHz		2.0		Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =15A		23.6		nC
Gate-Source Charge	Q _{gs}			3.9		
Gate-Drain Charge	Q _{gd}			7		
Reverse Recovery Charge	Q _{rr}	I _r =25A, di/dt=100A/us		0.2		ns
Reverse Recovery Time	t _{rr}			5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _L =1Ω R _{GEN} =3Ω		7		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			24		
Turn-off fall Time	t _f			24		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DD}=25V, V_G=10V, L=0.5mH, I_{AS}=14A

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

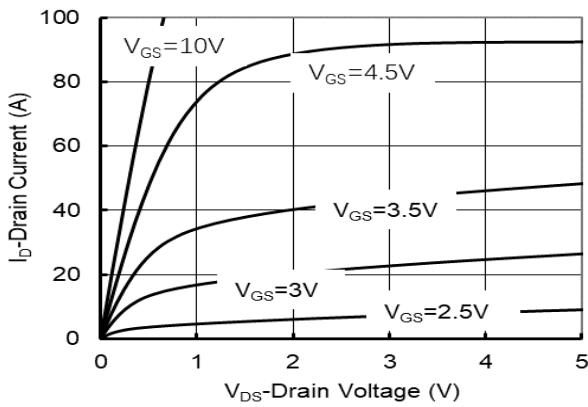


Figure1. Output Characteristics

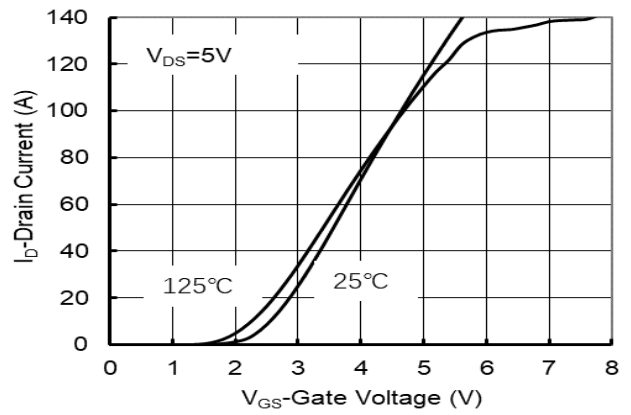


Figure2. Transfer Characteristics

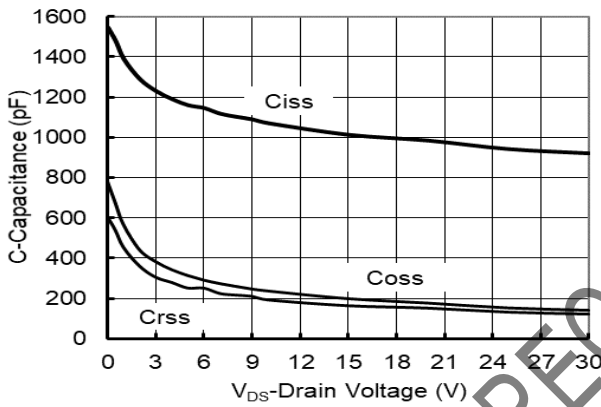


Figure3. Capacitance Characteristics

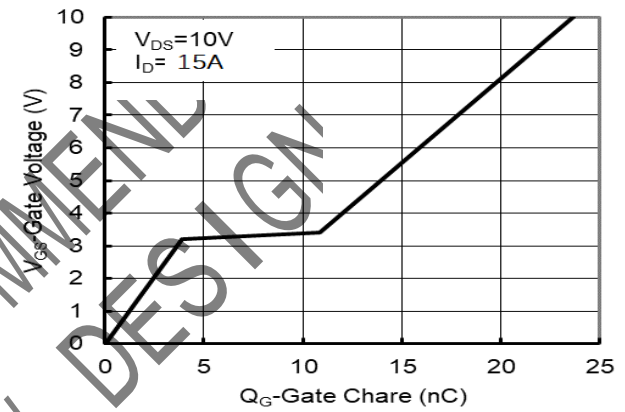


Figure4. Gate Charge

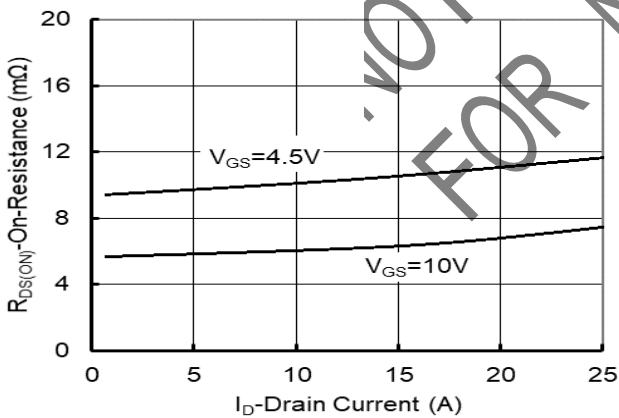


Figure5. Drain-Source on Resistance

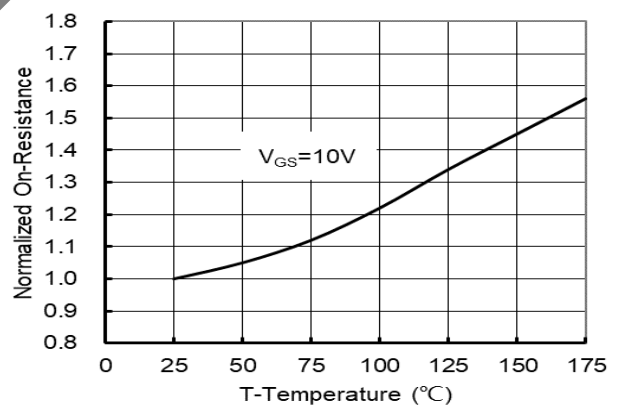


Figure6. Drain-Source on Resistance

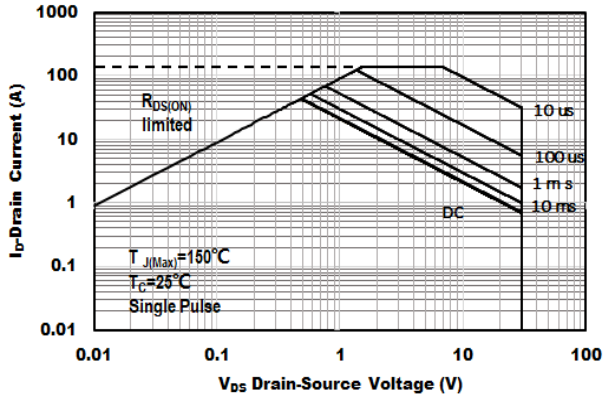


Figure7. Safe Operation Area

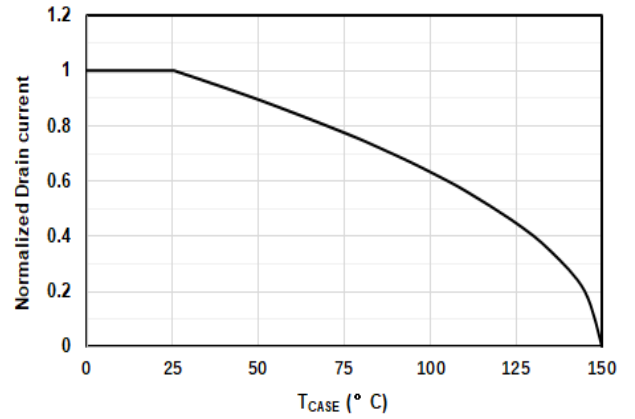


Figure8. Drain current vs. Case Temperature

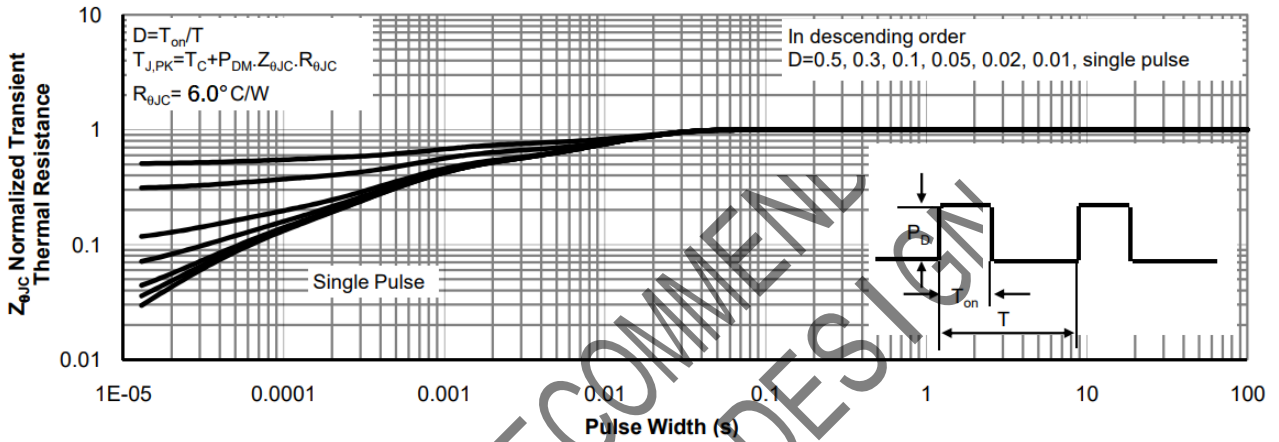
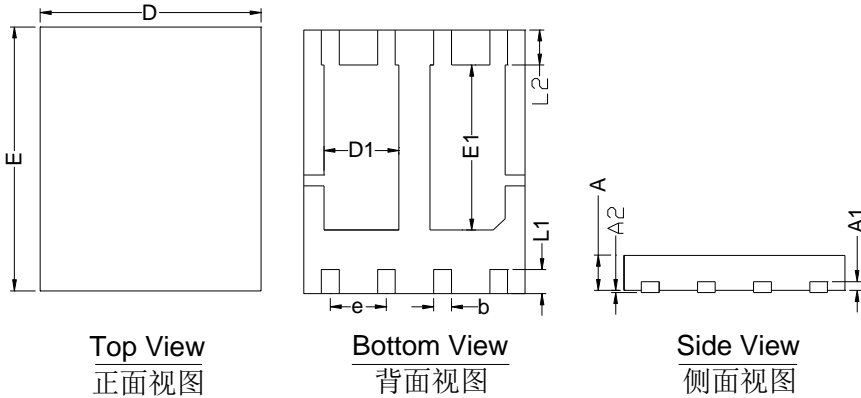


Figure 9. Normalized Maximum Transient Thermal Impedance

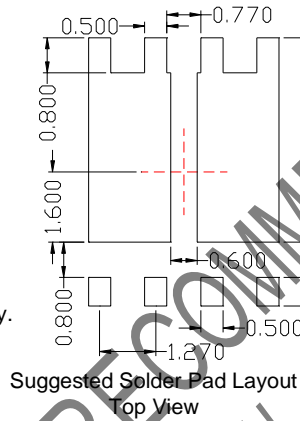


■ DFN5060-8L Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2	0.80 BSC		
b	0.30	0.40	0.50
e	1.27 BSC		

- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



NOT RECOMMEND
FOR NEW DESIGN



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