

## N-Channel and P-Channel Complementary MOSFET

### Product Summary NMOS

- $V_{DS}$  20V
- $I_D$  0.8A
- $R_{DS(ON)}$  ( at  $V_{GS}=4.5V$  ) < 300m $\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=2.5V$  ) < 400m $\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=1.8V$  ) < 950m $\Omega$
- ESD Protected Up to 2.0KV (HBM)

### PMOS

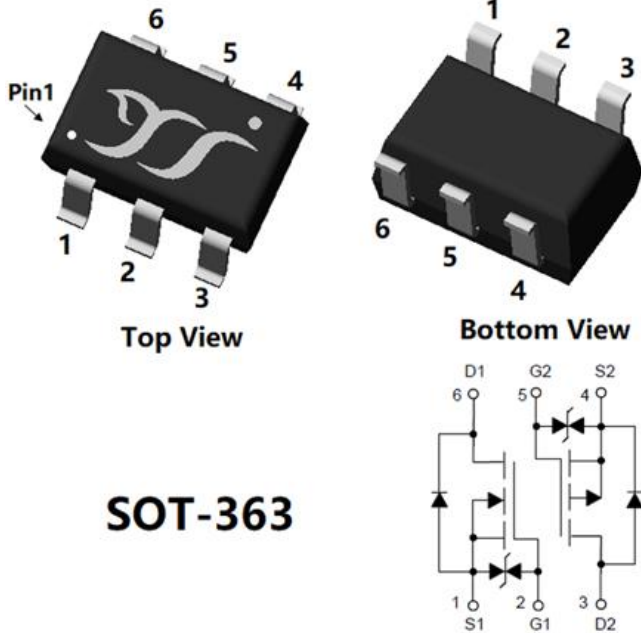
- $V_{DS}$  -20V
- $I_D$  -0.5A
- $R_{DS(ON)}$  ( at  $V_{GS}=-4.5V$  ) < 850m $\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=-2.5V$  ) < 1200m $\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=-1.8V$  ) < 2000m $\Omega$
- ESD Protected Up to 2.0KV (HBM)

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Interfacing, Logic switch
- Load switch
- Power management



### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		$V_{DS}$	20	-20	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	$\pm 10$	V
Drain Current	$T_A=25^\circ C$	$I_D$	0.8	-0.5	A
	$T_A=100^\circ C$		0.5	-0.3	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	3	-2	A
Total Power Dissipation <sup>B</sup>	$T_A=25^\circ C$	$P_D$	0.29	0.27	W
	$T_A=100^\circ C$		0.11	0.1	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient <sup>C</sup>	Steady-State	$R_{\theta JA}$	350	420	380	460	$^\circ C/W$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3439KADW	F2	49KA	3000	30000	120000	7" reel



# YJL3439KADW

## ■ NMOS Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V	-	-	±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.5A	-	210	300	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.4A	-	280	400	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =0.2A	-	406	950	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =0.8A, V <sub>GS</sub> =0V	-	-	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	37	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	0.8	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz	-	29	-	pF
Output Capacitance	C <sub>oss</sub>		-	11	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	5.4	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, I <sub>D</sub> =0.5A	-	2.17	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.25	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.23	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =0.5A, di/dt=100A/us	-	0.6	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	12	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, I <sub>D</sub> =0.5A R <sub>GEN</sub> =3Ω	-	2	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	17	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	14	-	
Turn-off fall Time	t <sub>f</sub>		-	26	-	



# YJL3439KADW

## ■ PMOS Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V	-	-	±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.5A	-	640	850	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.3A	-	900	1200	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-0.2A	-	1400	2000	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-0.5A, V <sub>GS</sub> =0V	-	-	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	75	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	-0.5	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz	-	37	-	pF
Output Capacitance	C <sub>OSS</sub>		-	12	-	
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	6	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.5A	-	2.55	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.35	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.31	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-0.5A, di/dt=100A/us	-	1.2	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	18	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-10V, I <sub>D</sub> =-0.5A R <sub>GEN</sub> =3Ω	-	3	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	18	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	20	-	
Turn-off fall Time	t <sub>f</sub>		-	27	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub>=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## ■ NMOS Typical Electrical and Thermal Characteristics Diagrams

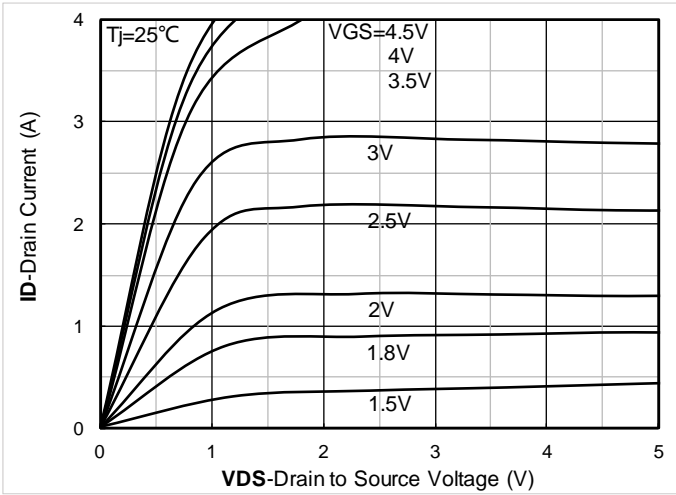


Figure 1. Output Characteristics

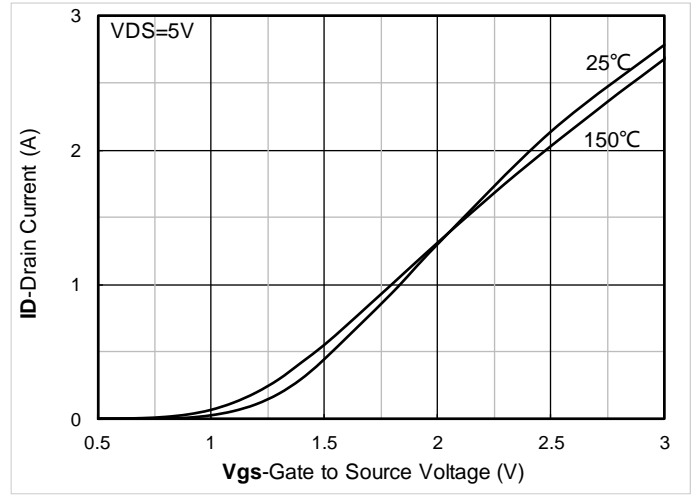


Figure 2. Transfer Characteristics

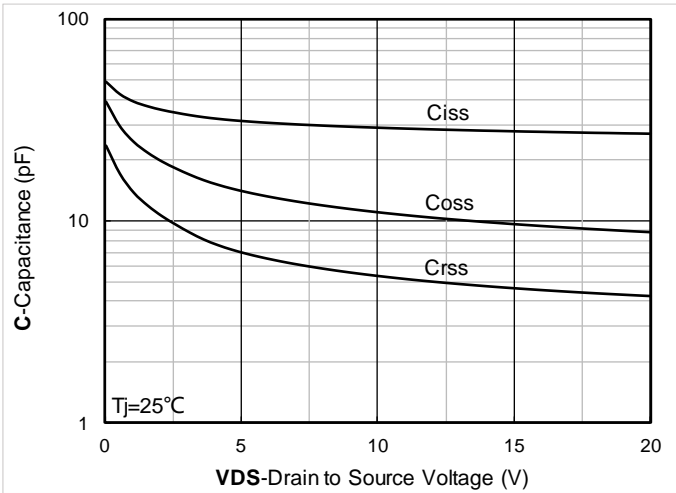


Figure 3. Capacitance Characteristics

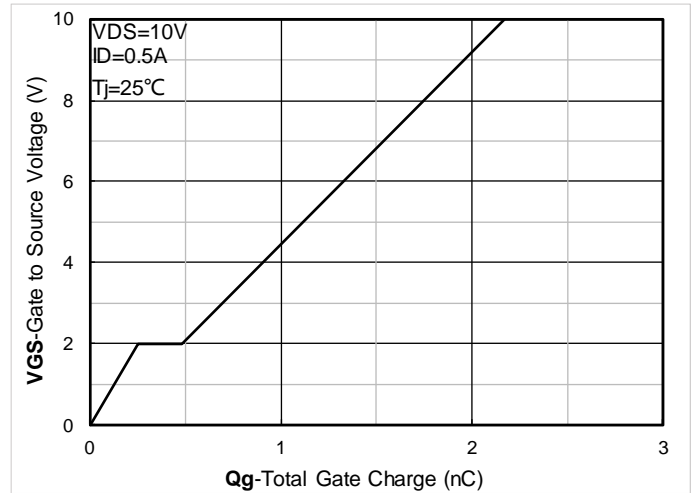


Figure 4. Gate Charge

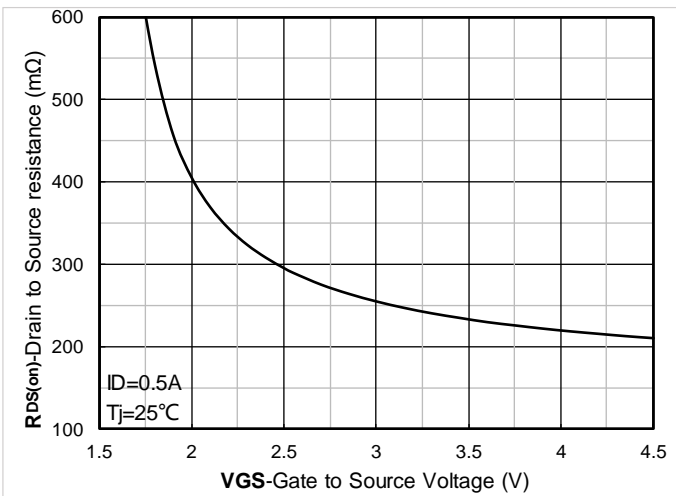


Figure 5. On-Resistance vs Gate to Source Voltage

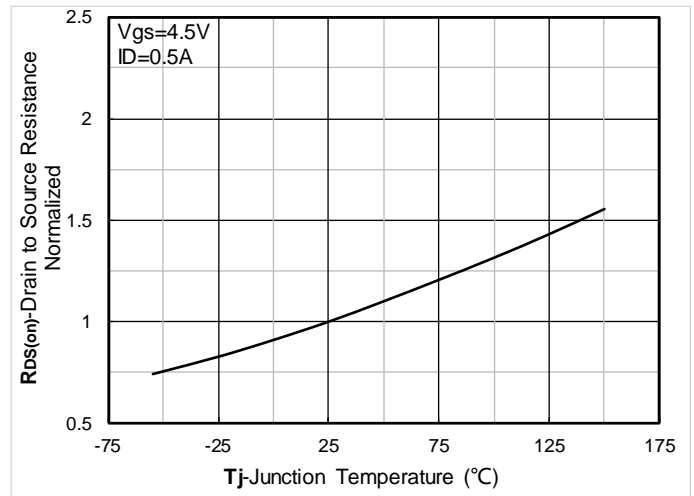


Figure 6. Normalized On-Resistance

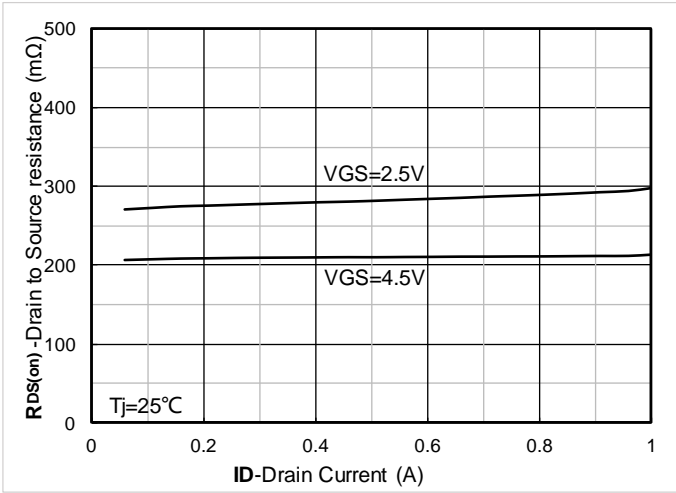


Figure 7.  $R_{DS(on)}$  VS Drain Current

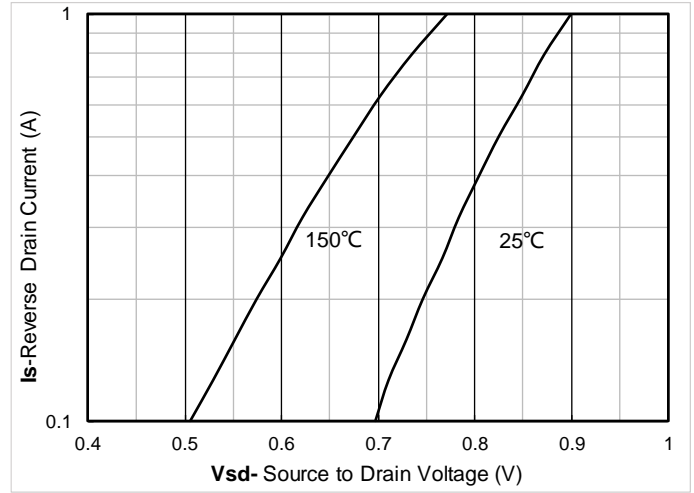


Figure 8. Forward characteristics of reverse diode

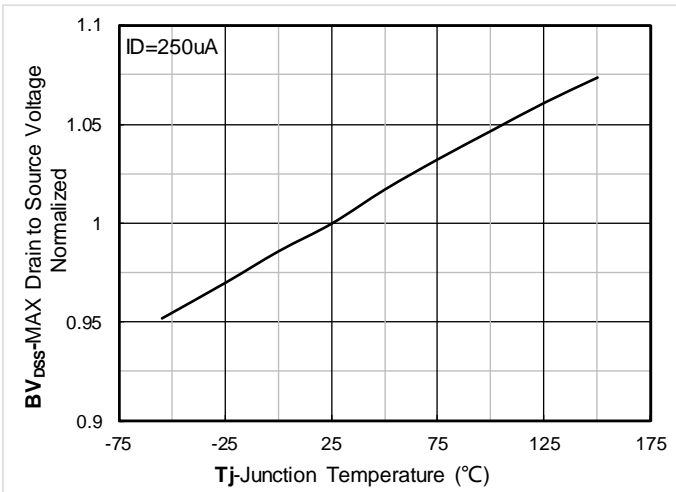


Figure 9. Normalized breakdown voltage

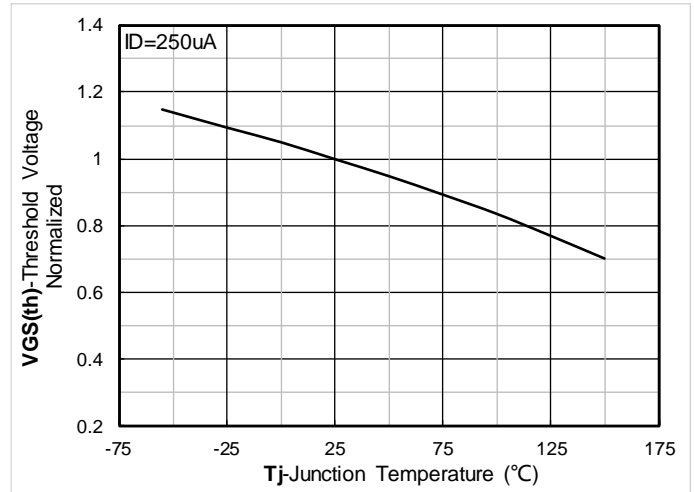


Figure 10. Normalized Threshold voltage

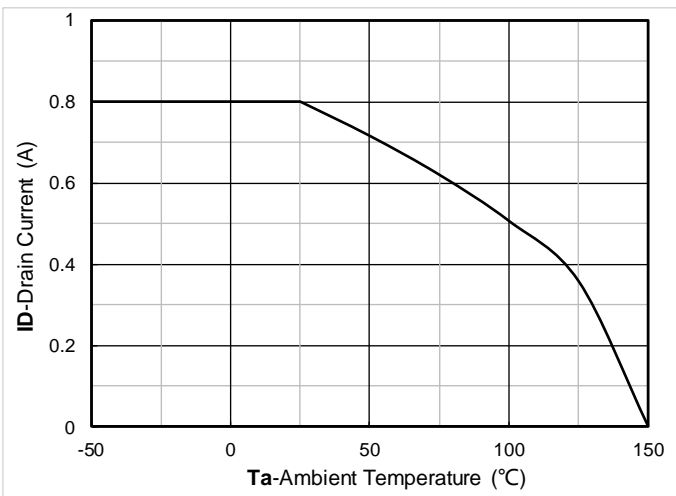


Figure 11. Current dissipation

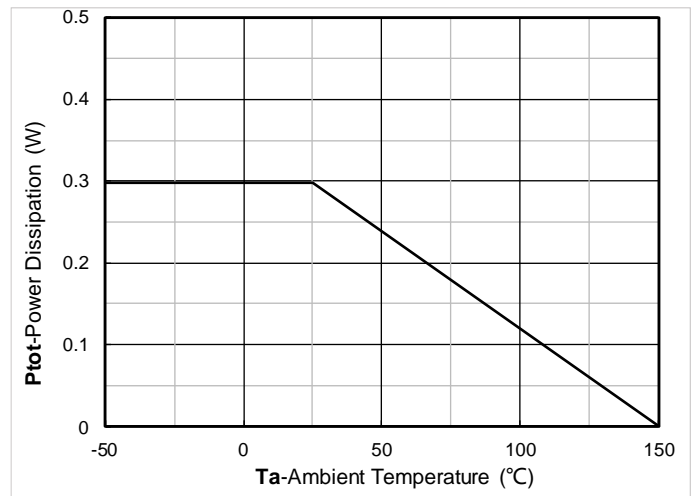


Figure 12. Power dissipation

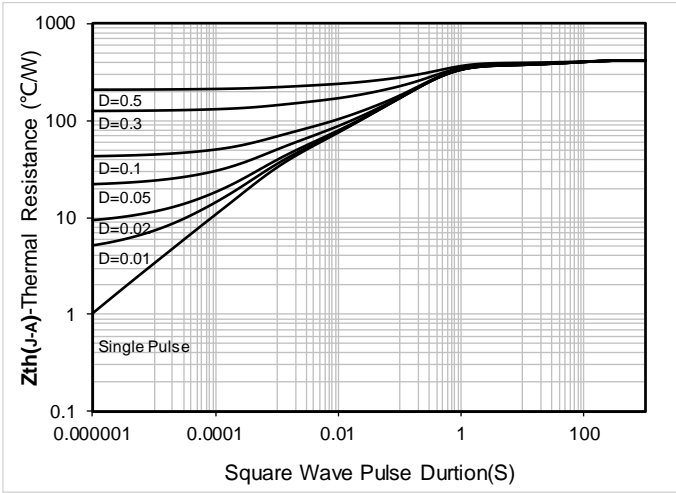


Figure 13. Maximum Transient Thermal Impedance

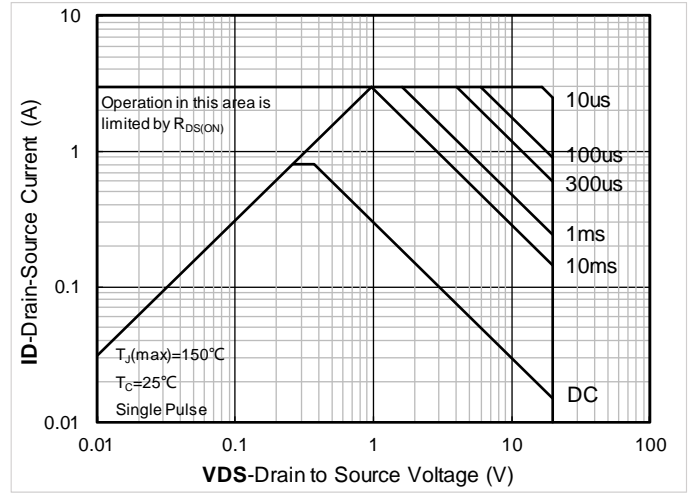


Figure 14. Safe Operation Area

## PMOS Typical Electrical and Thermal Characteristics Diagrams

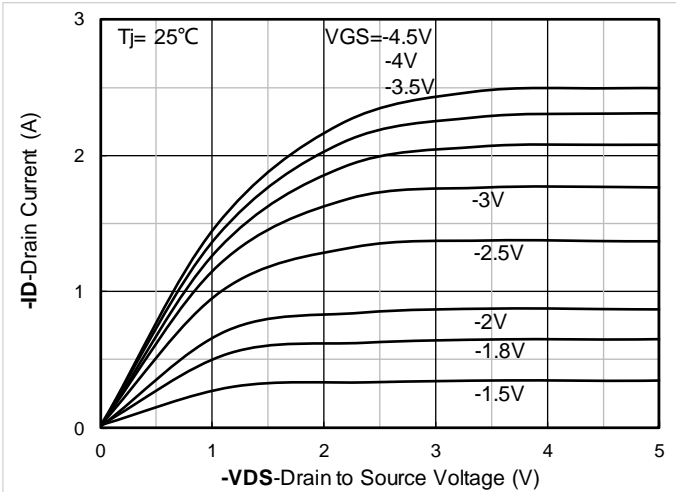


Figure 1. Output Characteristics

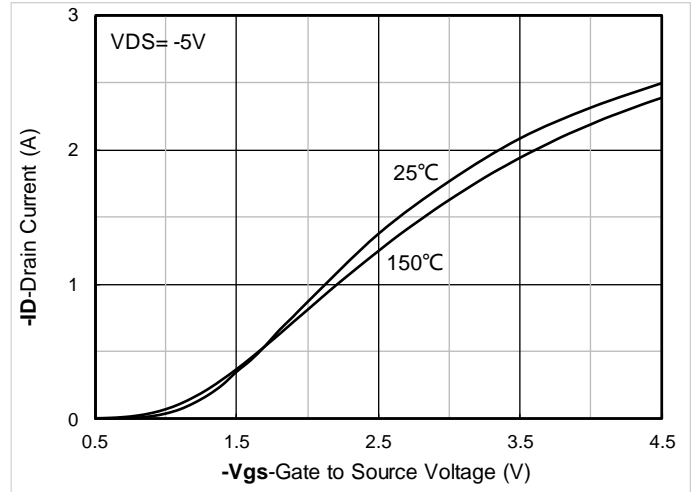


Figure 2. Transfer Characteristics

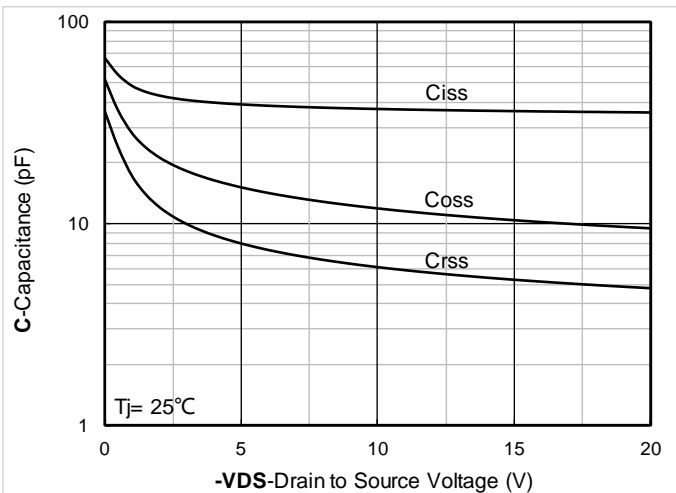


Figure 3. Capacitance Characteristics

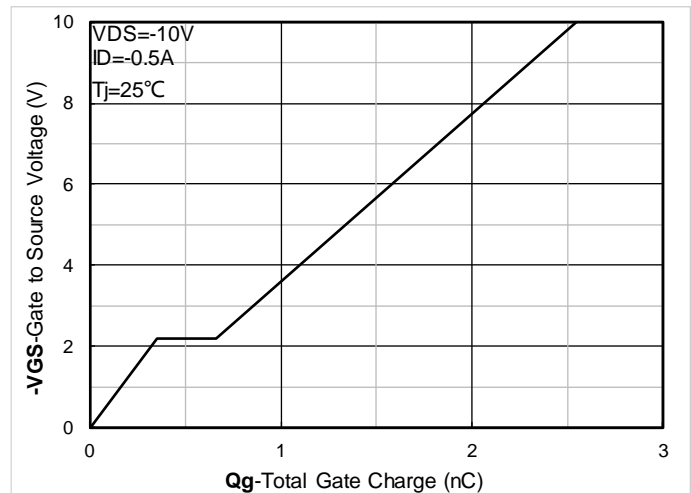


Figure 4. Gate Charge



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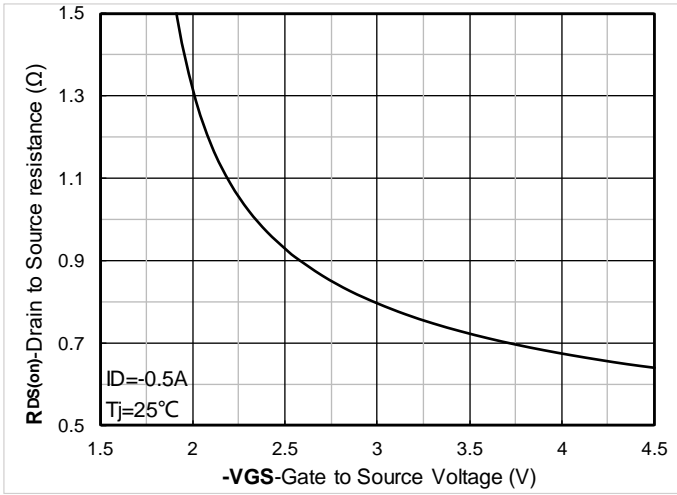


Figure 5. On-Resistance vs Gate to Source Voltage

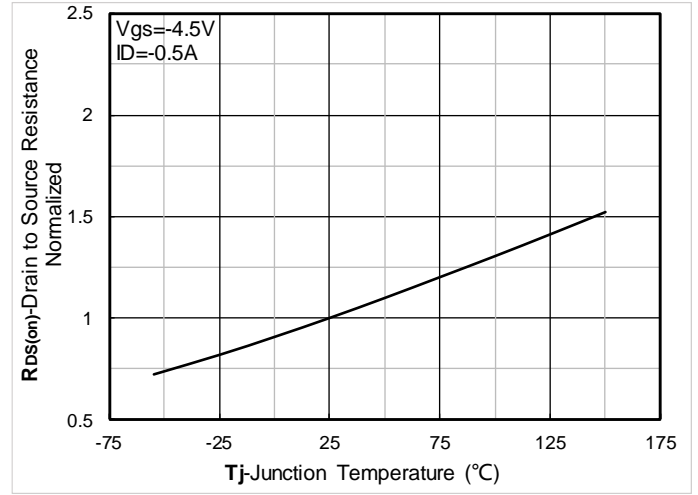


Figure 6. Normalized On-Resistance

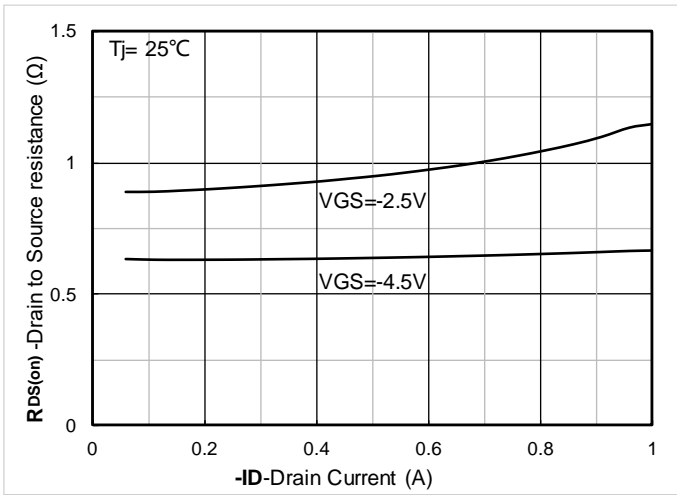


Figure 7. RDS(on) VS Drain Current

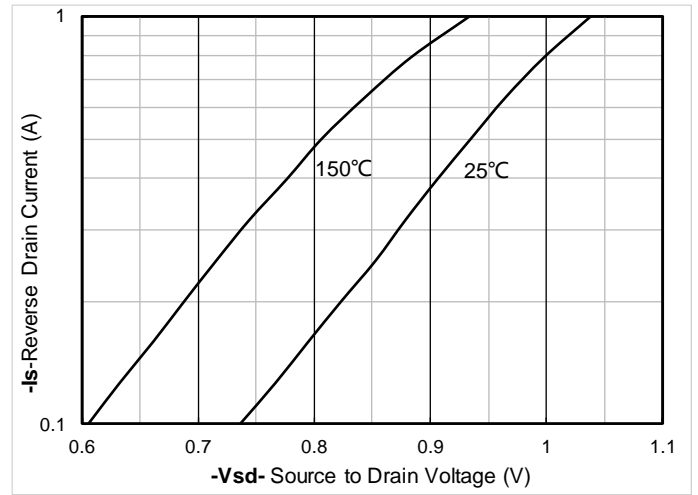


Figure 8. Forward characteristics of reverse diode

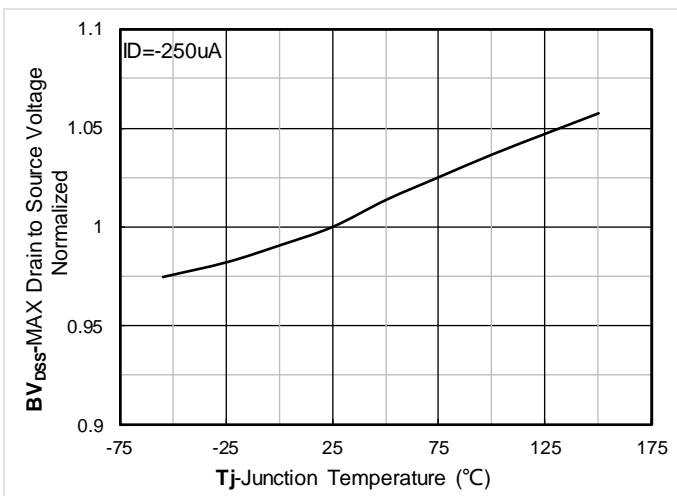


Figure 9. Normalized breakdown voltage

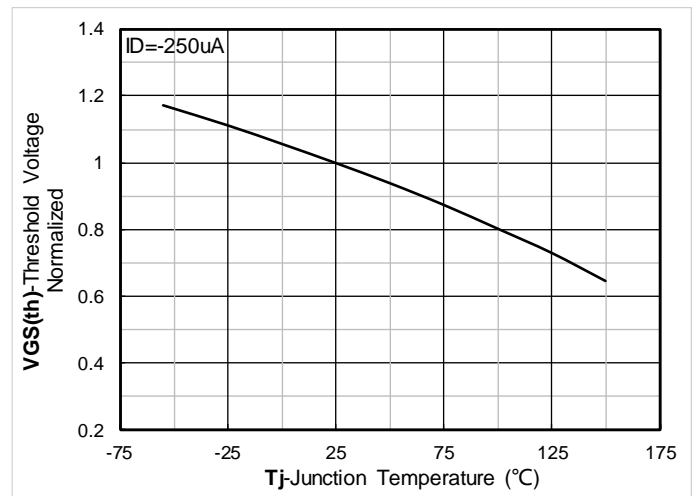


Figure 10. Normalized Threshold voltage



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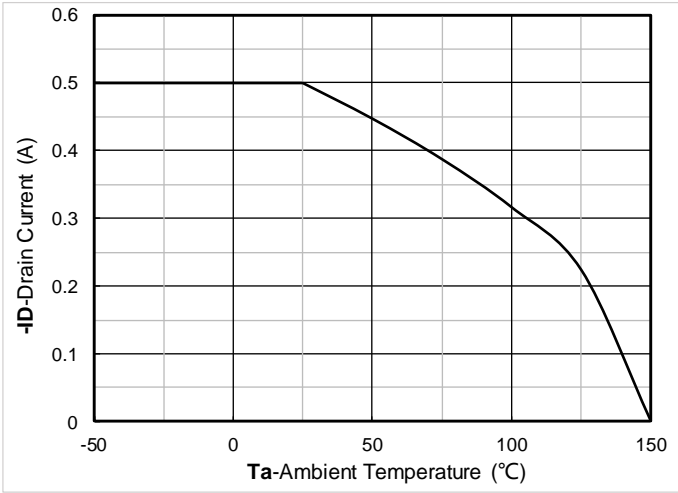


Figure 11. Current dissipation

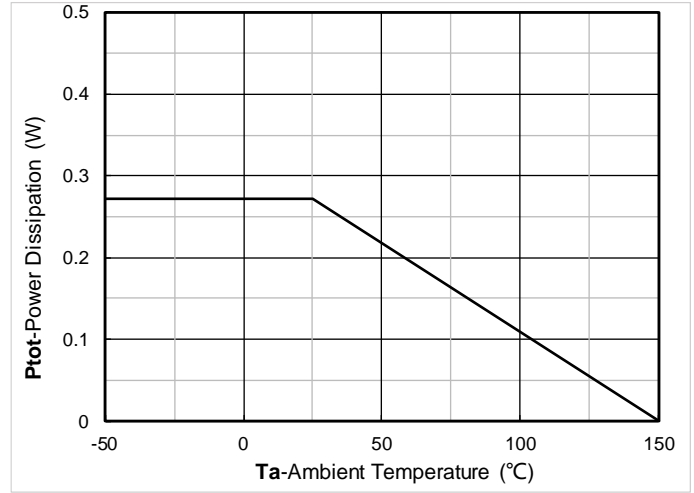


Figure 12. Power dissipation

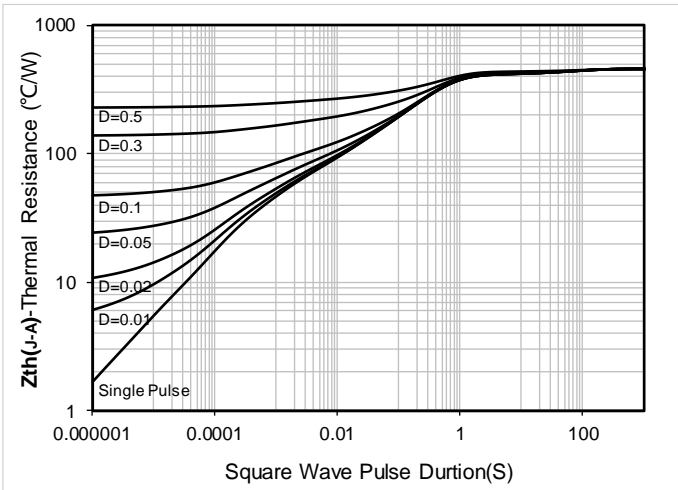


Figure 13. Maximum Transient Thermal Impedance

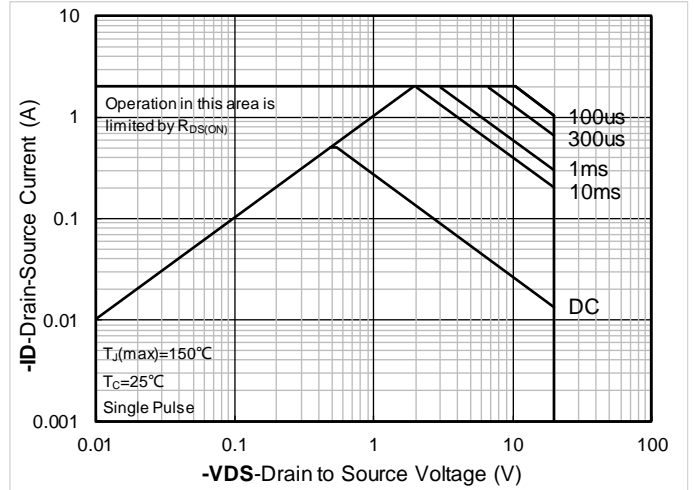
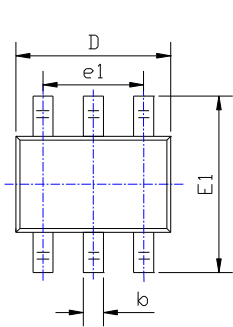


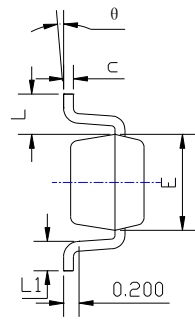
Figure 14. Safe Operation Area



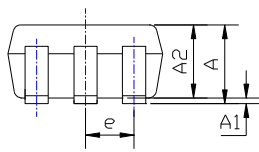
## ■ SOT-363 Package information



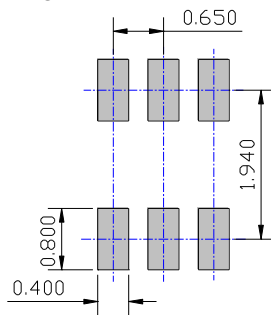
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.014	0.150	0.350
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026TYP		0.650TYP	
e1	0.047	0.055	1.200	1.400
L	0.021REF		0.525REF	
L1	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

**NOTE:**

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.

2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJL3439KADW

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### Disclaimer

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