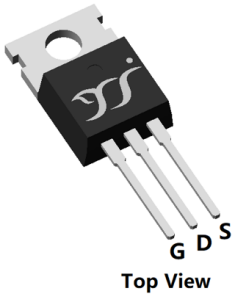
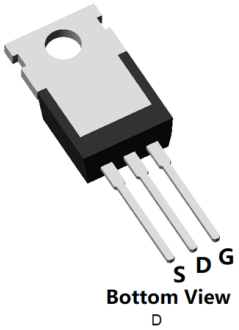
N-Channel Enhancement Mode Field Effect Transistor

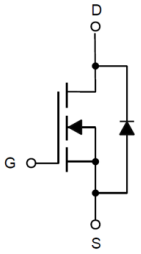


Top View



Bottom View

TO-220



Product Summary

- V_{DS} 200V
- I_D 95A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜11.5mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- UPS and Inverter applications
- Motor drivers
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	200	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}= 10V	I_D	-	11	A
		T_A=100℃,V_{GS}= 10V		-	7.8	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}= 10V,Chip limitation		-	95	
		T_C=100℃,V_{GS}= 10V		-	67	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	380	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		95	
Avalanche energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=0.5mH,IAS=50A		EAS	-	625	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	3.7	W
		T_A=100℃		-	1.8	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	277	
		T_C=100℃		-	138	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	40	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.54	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJP012G20H	B1	YJP012G20H	50	/	5000	Tube

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	200	-	-	V
		V_{GS}=0V,I_D=10mA,Tj=25℃	200	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=200V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	9.7	11.5	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.85	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	0.8	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V,f=1MHz,Tj=25℃	-	3920	-	pF
Output Capacitance	C_{oss}		-	445	-	
Reverse Transfer Capacitance	C_{rss}		-	11.3	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=100V,I_D=50A,Tj=25℃	-	50.5	-	nC
Gate-Source Charge	Q_{gs}		-	18.4	-	
Gate-Drain Charge	Q_{gd}		-	8.2	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V, V_R=100V,Tj=25℃	-	513	-	nC
Reverse Recovery Time	t_{rr}		-	135	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=100V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	20	-	ns
Turn-on Rise Time	t_r		-	42	-	
Turn-off Delay Time	$t_{D(off)}$		-	32	-	
Turn-off Fall Time	t_f		-	9	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

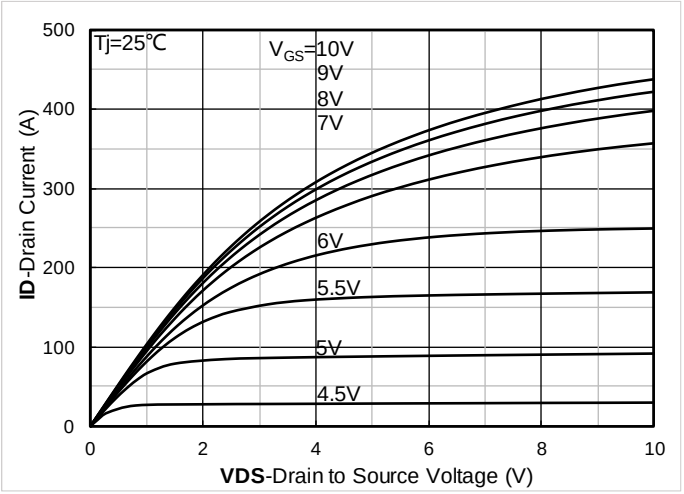


Figure 1. Output Characteristics; typical values

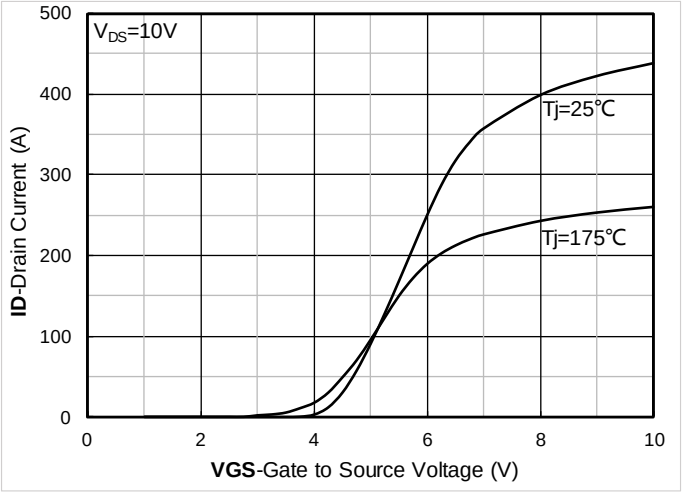


Figure 2. Transfer Characteristics; typical values

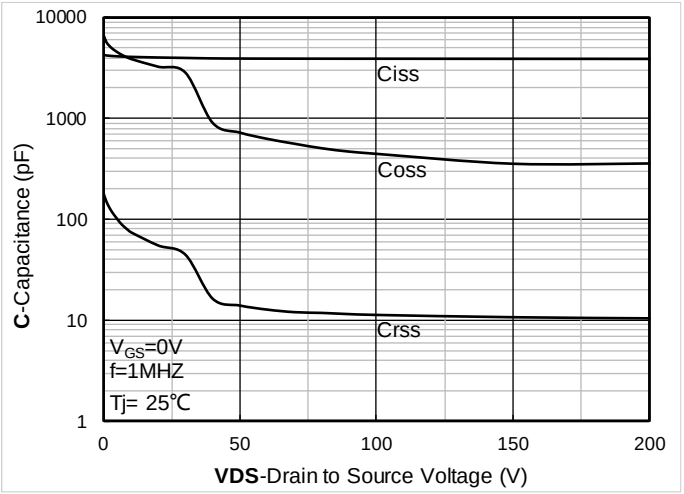


Figure 3. Capacitance Characteristics; typical values

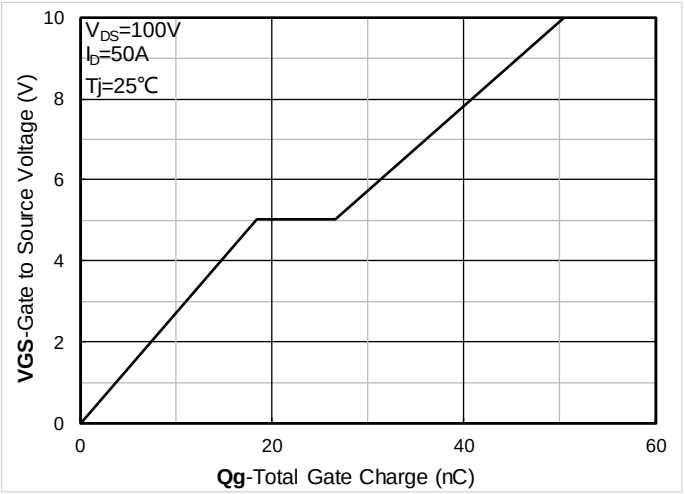


Figure 4. Gate Charge; typical values

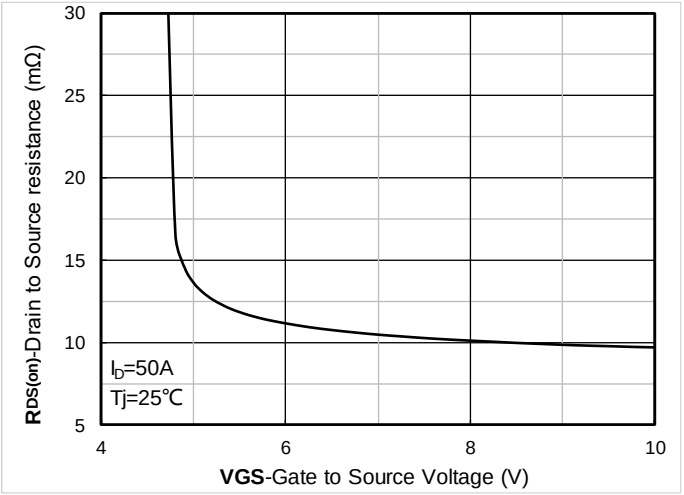


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

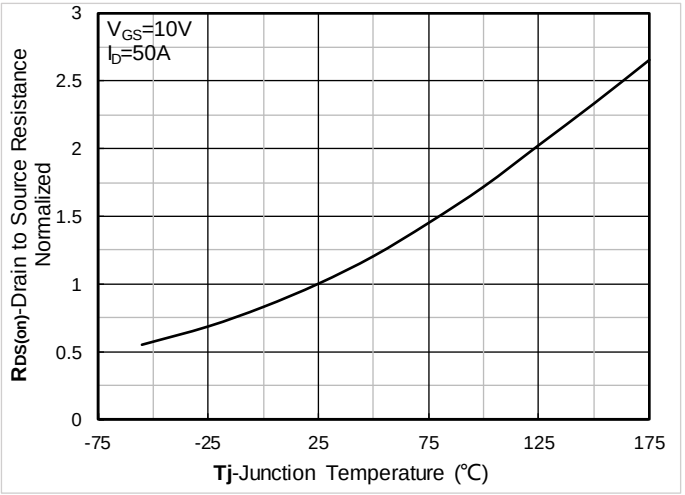


Figure 6. Normalized On-Resistance

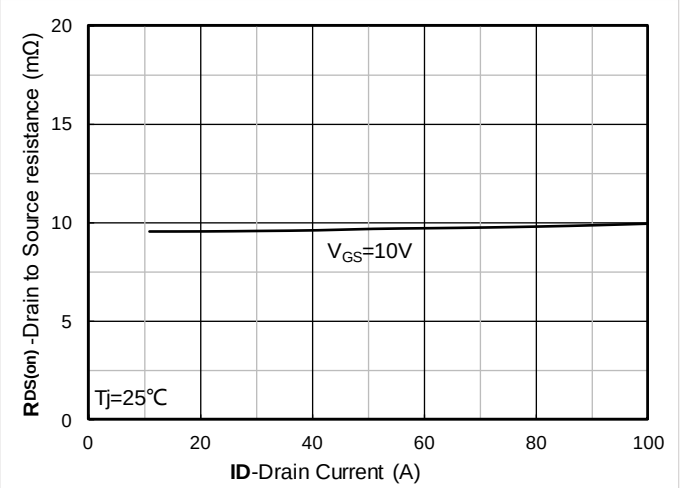


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

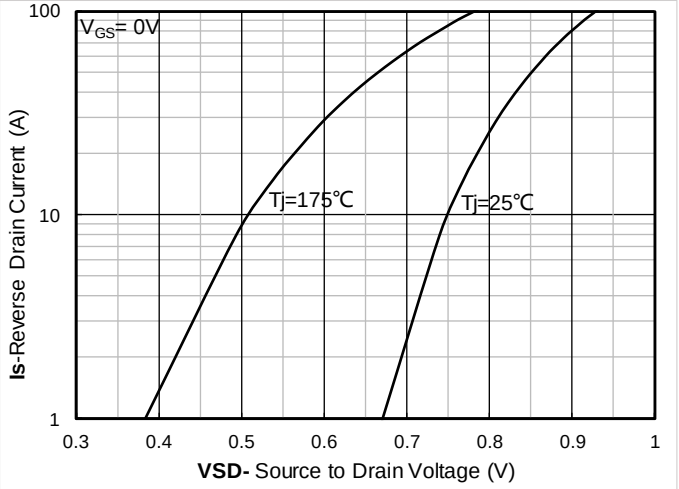


Figure 8. Forward characteristics of reverse diode; typical values

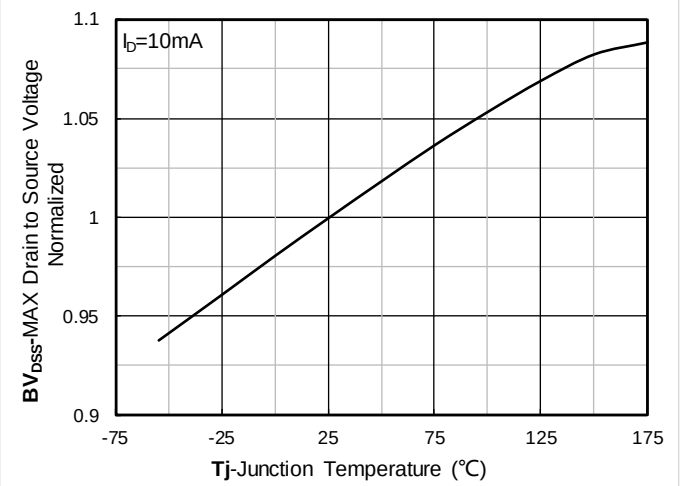


Figure 9. Normalized breakdown voltage

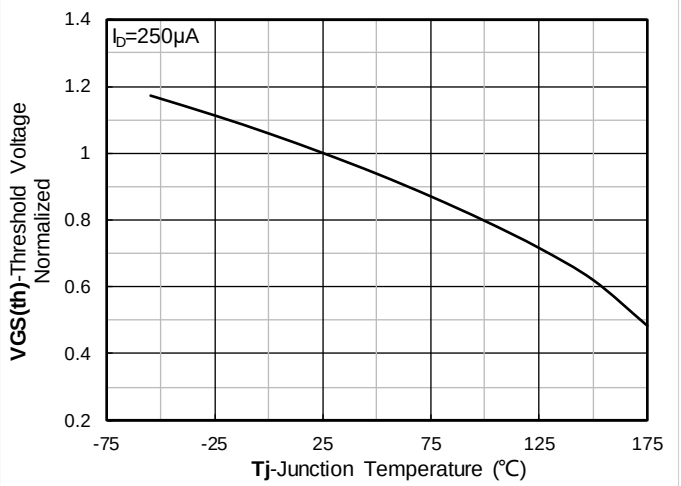


Figure 10. Normalized Threshold voltage

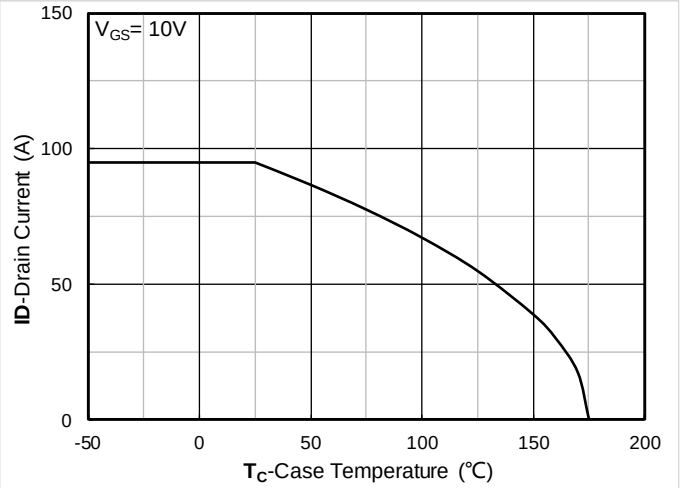


Figure 11. Current dissipation

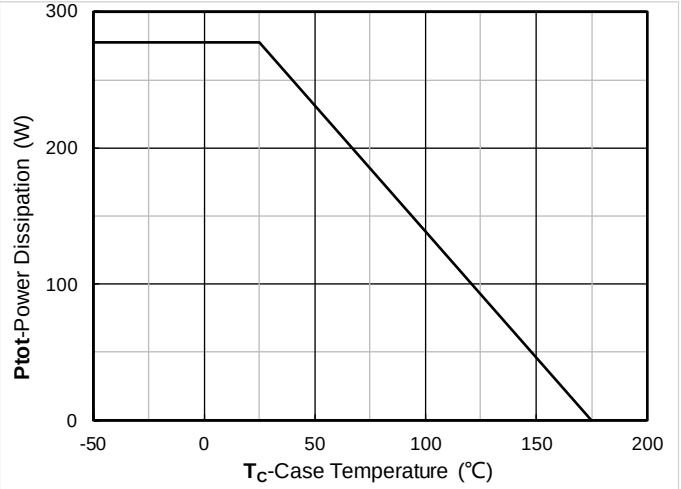


Figure 12. Power dissipation

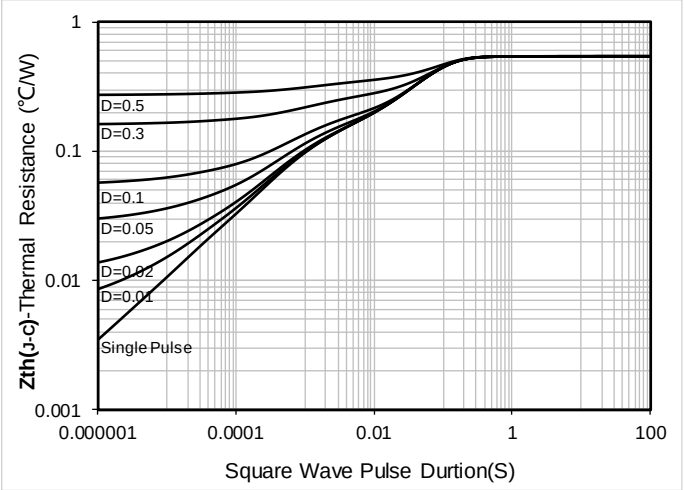


Figure 13. Maximum Transient Thermal Impedance

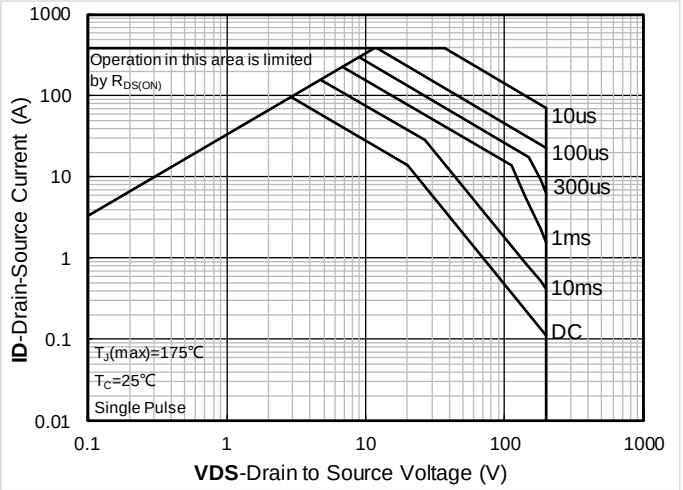


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

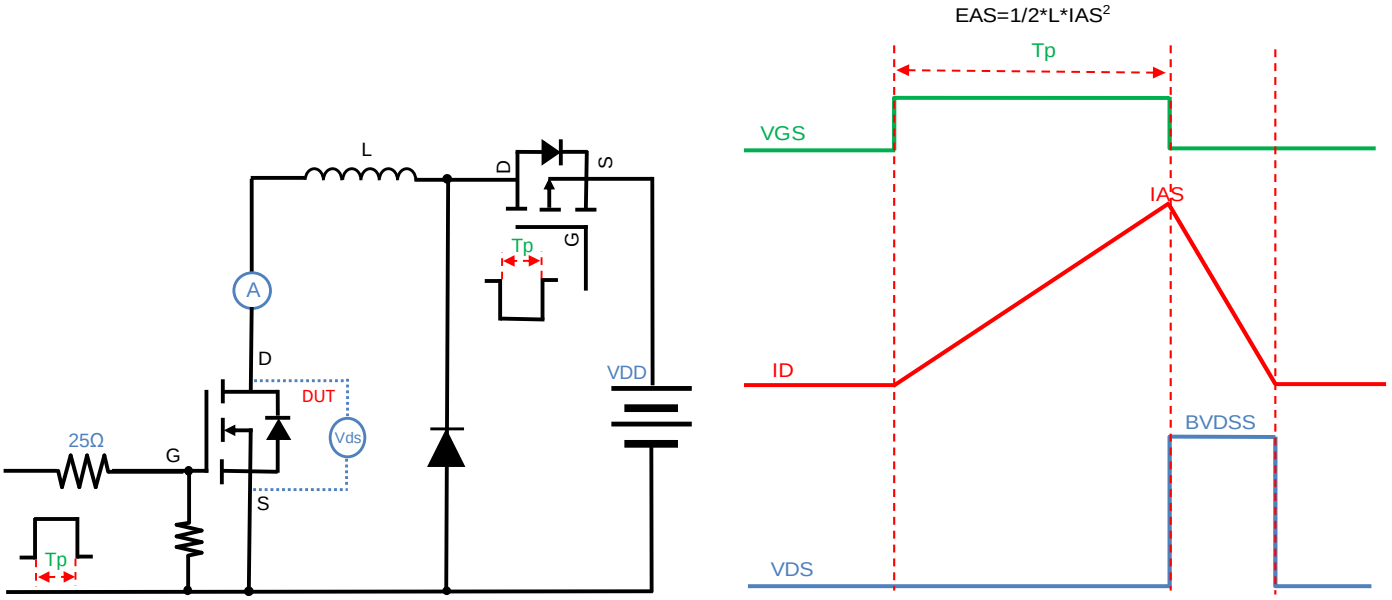


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

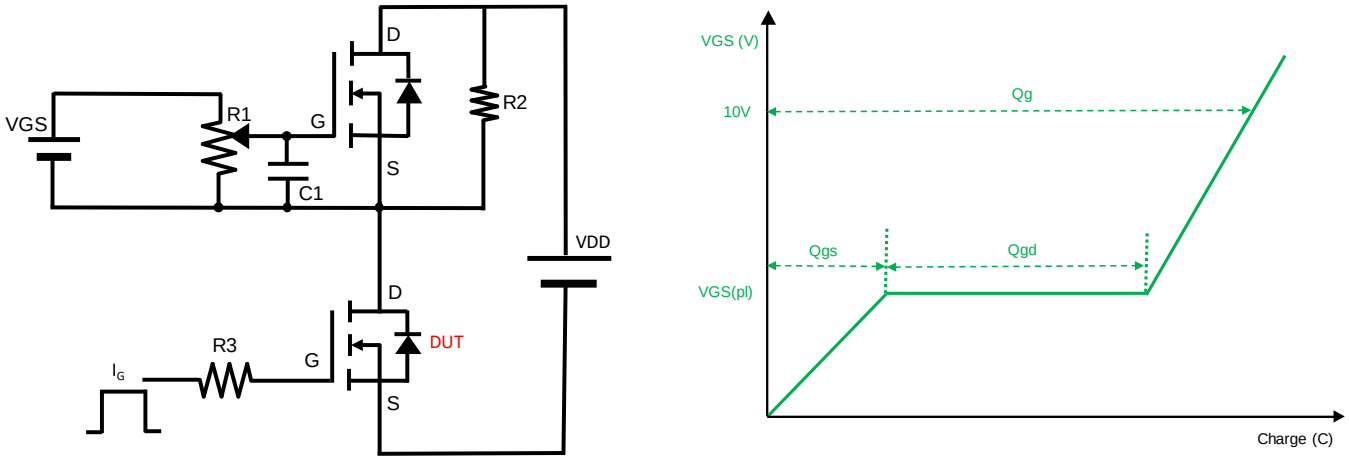


Figure B. Gate Charge Test Circuit & Waveform

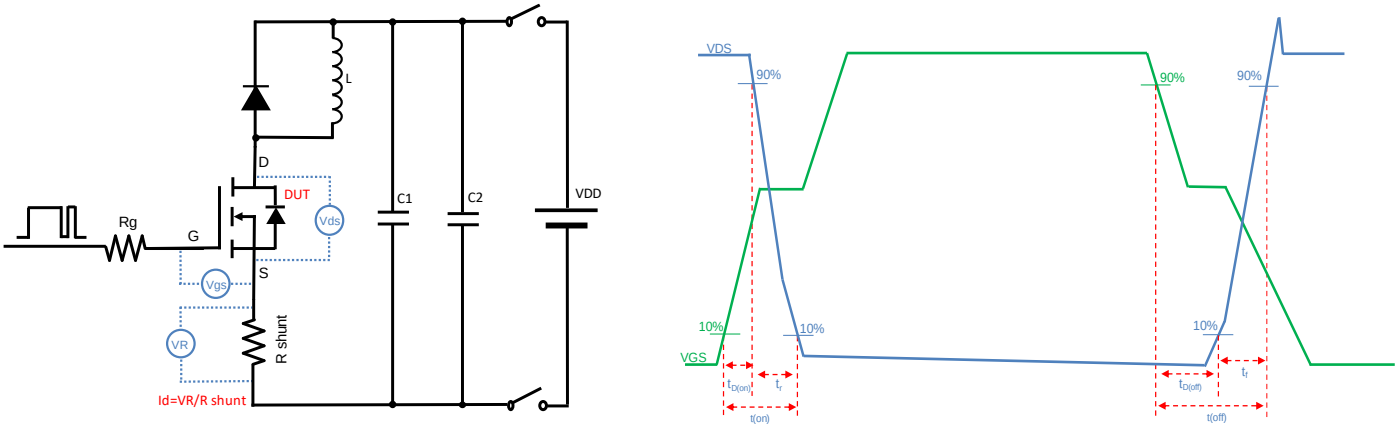


Figure C. Resistive Switching Test Circuit & Waveform

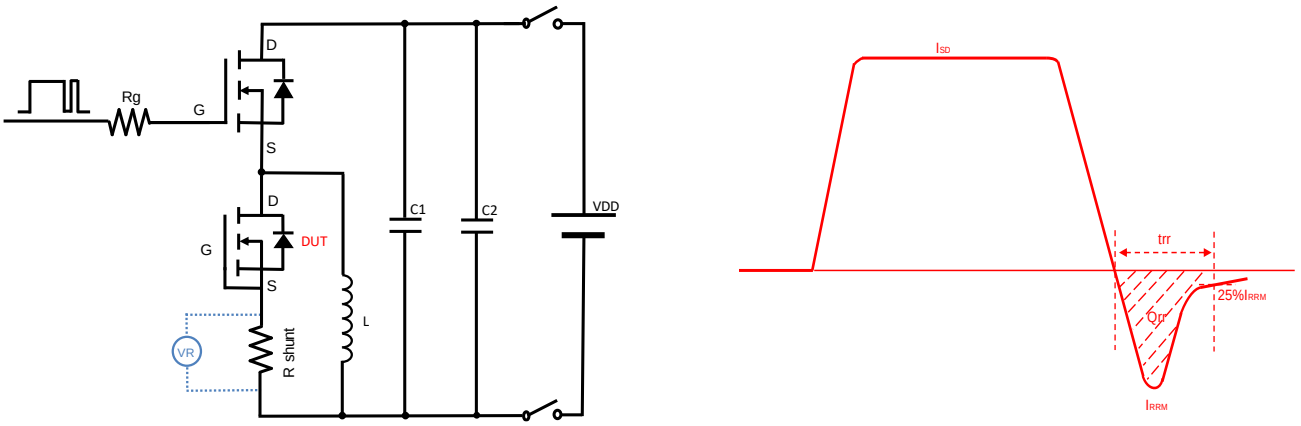
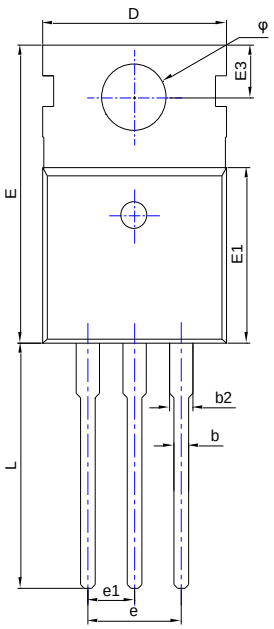
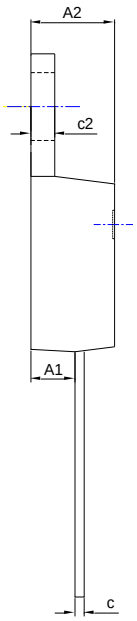


Figure D. Diode Recovery Test Circuit & Waveform

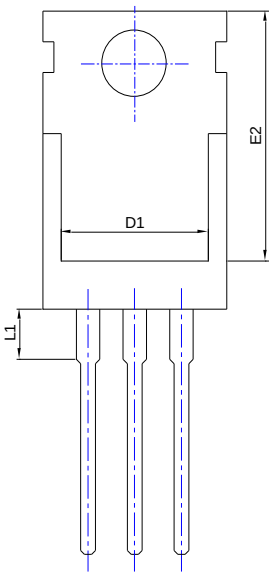
■ TO-220AB-E Package information



TOP VIEW



SIDE VIEW



BACK VIEW

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.093	0.114	2.350	2.900
A2	0.176	0.184	4.470	4.670
b	0.028	0.036	0.710	0.910
b2	0.048	0.054	1.220	1.360
c	0.019	0.024	0.470	0.600
c2	0.047	0.055	1.200	1.400
D	0.382	0.408	9.700	10.370
D1	0.276	0.350	7.000	8.890
E	0.579	0.622	14.700	15.800
E1	0.350	0.373	8.900	9.470
E2	0.463	0.535	11.750	13.600
E3	0.108BSC		2.740BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.508	0.583	12.900	14.800
L1	0.100	0.151	2.540	3.840
φ	0.142	0.154	3.600	3.900

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

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